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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,872	09/13/2000	Hartmund Terletzki	00P7882US	7001
25962	7590	07/13/2004	EXAMINER	
SLATER & MATSIL, L.L.P. 17950 PRESTON RD, SUITE 1000 DALLAS, TX 75252-5793				NGUYEN, MINH T
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,872	TERLETZKI ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 30 April 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 2-30 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 2-8,10-14,16,17 and 19 is/are allowed.

6) Claim(s) 9,15,18,20-28 and 30 is/are rejected.

7) Claim(s) 29 is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 12 April 2002 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____

DETAILED ACTION

1. Applicant's amendment filed on 3/30/04 has been entered. Claims 2-30 are pending. The prior art rejections to claims 9, 15, 18, 20-28 and 30 are maintained for the reasons set forth below. This action is FINAL.

Claim Objections

2. Claim 9 is objected to because of the following informalities: line 4, "a first voltage level" should be changed to -- the first voltage level -- to clearly refer the term to the one recited on line 2 and to avoid antecedent basis problem.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9, 15, 18, 20-27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,181,165, issued to Hanson et al. (a copy of the reference is not provided because it is listed in the IDS (PTO-1449).

Note that the rejections are based on Fig. 1 which is prior art, and Fig. 1 is known before the filing date (March 9, 1998).

As per claim 9, Hanson discloses a level shifting circuit (Fig. 1), comprising:

a first reference node carrying a first voltage level (about 1V, reduced voltage, column 2, lines 18-20);

a second reference voltage node carrying a second voltage level (ground, column 1, line 40), clearly ground is different from 1V;

a third reference node carrying a third voltage level (VDD), it is clear that VDD is different than ground or 1V;

an input node to receive an input signal (IN), the input signal varying between the first voltage level and a second voltage level (from 1V to ground);

a first n-channel transistor (106) having a first source/drain region, a second source/drain region and a gate, the gate being coupled to the input node (IN);

a second n-channel transistor (108) having a first source/drain region coupled to the second source/drain region of the first n-channel transistor, a second source/drain region coupled to a second voltage level reference node (ground) and a gate coupled to a first enable signal node (ENABLE);

a first p-channel transistor (104) having a first source/drain region coupled to the first source/drain region of the first n-channel transistor, a second source/drain region and a gate coupled to the input node (IN);

a second p-channel transistor (102) having a first source/drain region coupled to the second source/drain region of the first p-channel transistor, a second source/drain region coupled to a third reference node (VDD) and a gate coupled to a second enable signal node (ENABLEN).

As per claim 15, the recited limitation is disclosed in column 1, lines 29-30.

As per claim 18, it is clear that the third voltage level (VDD) is greater than the first voltage level (1V, reduced voltage).

As per claim 20, Hansen discloses a level shifting circuit (Fig. 1) comprising:

a level-shifting section (FETs 104 and 106) responsive to an input logic signal (IN), the input logic signal varying between a first voltage level (ground) and a second voltage level (1V, reduced voltage, column 2, lines 18-19), the level-shifting section providing an output logic signal (OUT), the output logic signal varying between the first voltage level (ground) and a third voltage level (reduced VDD), the third voltage level being different than the second voltage level (because $VDD \neq 1V$);

a first reference voltage node carrying a voltage at the first voltage level (ground);

a third reference voltage node carrying the third voltage level (reduced VDD); and

an enable/disable section (FETs 102 and 108) including a first portion (FET 108) coupled between the level shifting section and the first reference voltage node (ground) and a second portion (FET 102) coupled between the level shifting section and the third reference voltage node (VDD), the enable/disable section being responsive to an enable/disable signal

(ENABLE/ENABLEN), the enable/disable section causing the output terminal to be placed at a relatively high output impedance condition independent of the logic state of the input logic signal

in response to a disable mode indication from the enable/disable signal (column 1, lines 30-33, tri-state).

As per claim 21, VDD or 1V represent logic “HI” and ground represents logic “LOW”.

As per claim 22, the recited first transistor reads on FET 104 and the recited second transistor reads on FET 106.

As per claim 23, the recited third transistor reads on FET 102 and the recited fourth transistor reads on FET 108.

As per claim 24, disclosed in column 1, lines 29-33.

As per claim 25, the recited first switch reads on FET 108 and the recited second switch reads on FET 102.

As per claims 26-27, since ENABLEN is inverted of ENABLE (column 1, lines 29-30), the recited limitations are inherently met.

As per claim 30, (102) and (108) are MOS transistors.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,181,165, issued to Hanson et al.

Hanson discloses a level shifting circuit having the structure discussed in claim 26 but he does not explicitly disclose the inverter is powered by the power supply voltage VDD.

As known by a person skilled in the art, the inverter in the Hanson circuit can be powered by the VDD or the reduced voltage, and using VDD to power the inverter, FETs 102 and 108 can be functioned more like switches because smaller voltage drop across the drain and source of the FETs, i.e., recall the basic operation of a FET, when a FET is used as a switch, the FET should be operated in saturation mode.

It would have been obvious to one skilled in the art at the time of the invention was made to power the inverter using VDD voltage instead of the reduced voltage to improve the output swing of the OUT signals.

Response to Arguments

5. Applicant's arguments filed 4/30/04 have been fully considered but they are not persuasive.

Regarding the argument in the Hanson's circuit of Figure 1, when the input voltage is reduced, the output voltage also reduced. The reference simply never teaches a case where the input carries a reduced voltage and the output carries a full voltage (Vdd). Therefore, the reference does not teach or suggest the limitations of claim 9.

The argument is not clear because the Applicant does not explicitly point out which limitation is not taught. It appears the Applicant is trying to argue the output must carry a full supply voltage (Vdd) in order for the reference anticipates claim 9. If this is the case, the examiner would like to point out that the claim does not require the output voltage must be Vdd.

Regarding the argument there is no indication the Hanson's circuit of Figure 1 can provide any level shifting capabilities as required by claim 9.

As discussed in the preceding rejections, the examiner explicitly points out every limitation recited in the claim is met by the Hanson's reference, the Hanson's circuit must be assumed to provide the level shifting capabilities. The examiner further points out that MPEP 2112.01 explicitly discusses about this point and cited various court cases to support the point, the Applicant is invited to study and compare with the instant issue. In this instant case, the Hanson's circuit of Figure 1 teaches all the structure as discussed, the claim properties must be assumed to be inherent and the *prima facie* case of anticipation is established.

Regarding the argument Hanson does not teach the output logic signal varying between the first and third voltage levels when the input logic level varying between the first and second voltage levels wherein the third voltage level is different than the second voltage level as required by claim 20.

The applicant is invited to consider the second situation where the input voltage vary between a reduced voltage and ground. Specifically, the input voltage varies between 0 and 1 volts with a supply voltage VDD of 5 volts at the source terminal of PMOS 102, it is clear that the output voltage would vary between 0 volt and a third voltage level which is clearly not equal to 1 volts. The fact is that when the input voltage is reduced to a value of less than the supply voltage VDD, MOSFETs 104 and 106 do not fully operated as switches by fully ON or OFF, therefore, the output voltage is reduced, however, it is not equal to the reduced input voltage.

Allowable Subject Matter

6. Claims 2-8, 10-14, 16-17 and 19 are allowed for the reasons noted in the previous Office actions.

7. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 29 is allowable for the same reason noted in claim 16.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



7/9/04

Minh Nguyen
Primary Examiner
Art Unit 2816